Audio Synthesizer Project Report

Titus Lee, Gary Park

***Abstract*—The goal of this project was to design and build an audio synthesizer using a fully discrete BJT-based operational amplifier powered by a 9 V supply. The circuit was designed to generate audible tones over a frequency range of approximately 260 Hz to 1040 Hz, with user control provided through two potentiometers. One potentiometer primarily controlled the oscillation frequency, while the other affected both the output amplitude and frequency due to the feedback configuration. The system was analyzed using hand calculations, verified through simulations, and implemented on a custom PCB. The final hardware successfully produced audible tones across the target frequency range and allowed the output volume to be adjusted over approximately a 10× range, meeting the primary objectives of the project.**

Author Contributions— Titus Lee focused on circuit simulations and experimental measurements, while Gary Park focused on hand analysis and PCB design and implementation. Both authors collaborated on circuit design decisions, debugging, and preparation of the final report.

I. Introduction

This project focuses on the design and implementation of an audio synthesizer built around a fully discrete BJT-based operational amplifier. Unlike integrated op-amps, the amplifier was constructed using individual transistors, including a differential input stage, a voltage gain stage, and a class-AB output stage, which allowed for direct control over biasing, gain, and stability. The op-amp was configured with both positive and negative feedback to operate as a relaxation oscillator, producing an audible output signal that could be adjusted by the user. Design constraints included operation from a single 9 V supply, the use of standard discrete BJTs, and the ability to directly drive an 8Ω speaker through an output buffer stage. The design process followed an iterative approach consisting of hand analysis, circuit-level simulation, printed circuit board (PCB) design, and experimental testing. The following sections present the analysis, simulation results, experimental measurements, and a discussion of the final system performance.

II. Hand Analysis

This section describes the hand analysis used to design the discrete BJT operational amplifier and its feedback network. The overall circuit is built around a custom op-amp core followed by a separate output buffer stage. The op-amp core consists of a PNP differential input stage, an NPN voltage gain stage with an active load, and a complementary class-AB output stage. Together with positive and negative feedback, this amplifier is configured as a relaxation oscillator that generates the audio signal. The oscillator output is then passed to a second unity-gain class-AB buffer to provide sufficient current to drive the 8Ω speaker. Hand calculations were used to set bias currents, estimate stage gains, and determine expected operating ranges before moving on to simulation and PCB implementation. The analysis is presented in a bottom-up manner, beginning with the differential input stage and progressing through the remaining stages and feedback network. For calculations, we assumed $V_D = 0.7V$, $\beta = 400$, $V_{CC}/V_{EE} = \pm 4.5V$, $r_{o,7} = 700k\Omega$, and $V_T = 25mV$. Additionally, $s = j\omega$.

This is the final project report for ECE 3660 Microelectronics, Fall 2025 at the University of Virginia

A. DC Bias Calculations

The DC operating point establishes the small-signal parameters of the circuit. The initial current set by the diode-configured Q_1 is:

$$I_D = \frac{V_{CC} - V_D}{R_1} \approx 210\,\mu A \tag{1}$$

Using the standard BJT small-signal relations,

$$\begin{aligned} g_m &= \frac{I_C}{V_T}, \\ r_d &= \frac{1}{g_m}, \\ r_\pi &= \frac{\beta}{g_m} \end{aligned} \tag{2}$$

the following parameters are obtained.

For diode-connected transistor Q_9:

$$\begin{aligned} g_{m,3} &= \frac{I_D}{V_T}, & r_{\pi,3} &= \frac{\beta}{g_{m,9}} \\ g_{m,9} &= \frac{I_D}{V_T}, & r_{d,9} &= \frac{1}{g_{m,9}} \\ g_{m,11} &= \frac{I_D}{V_T}, & r_{\pi,11} &= \frac{\beta}{g_{m,11}} \\ g_{m,13} &= \beta V_T, & r_{\pi,13} &= \frac{1}{g_{m,13}} \end{aligned} \tag{3}$$

B. Differential Input Stage

The differential input stage serves as the interface between the external input signals and the internal amplifier core. Its primary purpose is to sense the voltage difference between the two input nodes while rejecting any common-mode signal present at both inputs. This stage converts the differential input voltage into a single-ended signal that the subsequent stages can further amplify. Additionally, the differential pair

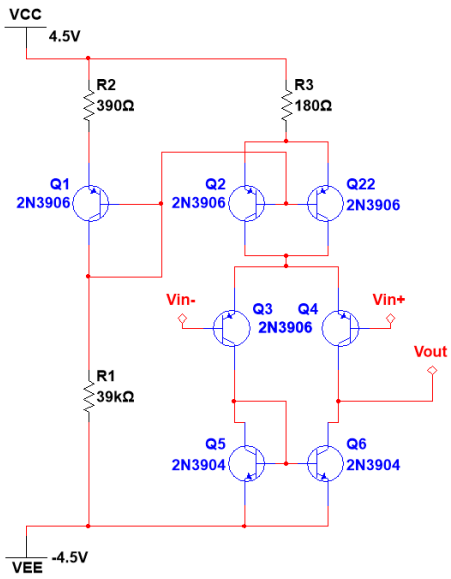

Fig. 1. Differential Input Stage Schematic

establishes a high input impedance. The values for R_2 and R_3 are chosen to allow more headroom for the amplifier.

$$A_{DM,L} = -2g_{m,3}R_{in,\text{2nd gain stage}}, \qquad Z_{in} = \frac{\beta}{g_{m,3}}, \qquad g_{m,3} = \frac{I_C}{V_T} \tag{4}$$

C. Voltage Gain Stage

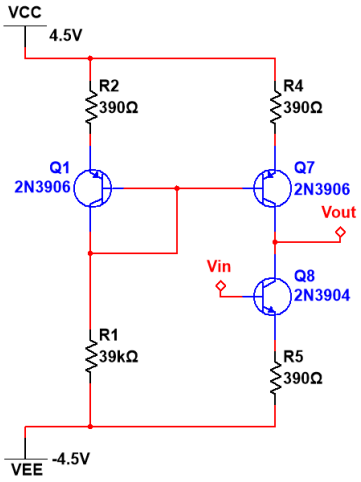

Fig. 2. Second Gain Stage Schematic

The voltage gain stage is responsible for generating the majority of the op-amp's open-loop gain. By converting the small differential signal from the input stage into a much larger voltage swing, this stage ensures that the amplifier has sufficient gain for effective feedback control. Using an active load increases the achievable gain while maintaining reasonable voltage headroom. This stage also defines the amplifier's dominant pole via the Miller capacitor (not shown—between the base and collector of Q_8), which stabilizes the system and prevents oscillations under negative feedback.

$$A_{OC} = -\left(\frac{g_{m,8}R_C}{1+\frac{\beta+1}{\beta}g_{m,8}R_5}\right)\left(\frac{1}{sR_CC_O+1}\right) \tag{5}$$

$$R_C = r_{o,7} + R_4 \tag{6}$$

$$C_O = C_F\left(1+\frac{1}{A_0}\right), \qquad C_M = C_F(1+A_0) \tag{7}$$

$$Z_{in} = \frac{r_{\pi,8}\left(1+\frac{\beta+1}{\beta}g_{m,8}R_5\right)}{sC_Mr_{\pi,8}\left(1+\frac{\beta+1}{\beta}g_{m,8}R_5\right)+1} \tag{8}$$

$$Z_{out} = \frac{r_o+R_4}{sC_O(r_o+R_4)+1} \tag{9}$$

D. Class-AB Output Buffer Stage

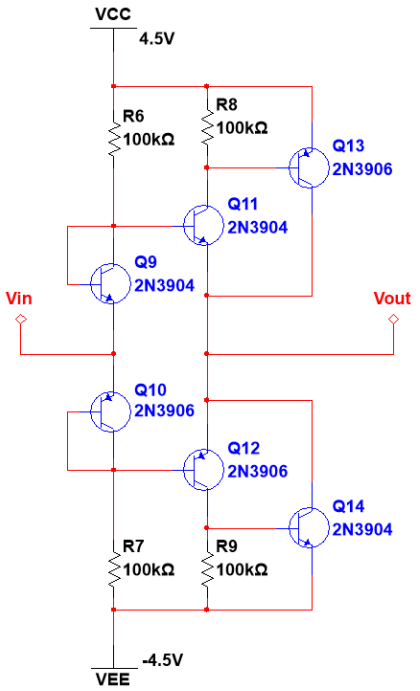

Fig. 3. Class AB Output Stage Schematic

The first class-AB output buffer, located immediately after the voltage gain stage, isolates the high-gain internal nodes from loading effects. Its primary function is to provide a high input impedance and low output impedance while maintaining approximately unity voltage gain. This buffering prevents the gain stage from being significantly affected by load variations and improves the overall linearity and stability of the op-amp.

To simplify the nodal equations, the following composite admittance terms are defined:

$$\alpha = \frac{1}{r_{d,9}} + \frac{1}{R_6} + \frac{1}{r_{\pi,11}}, \quad \delta = \frac{1}{R_7} + \frac{1}{r_{\pi,13}} \tag{10}$$

The overall small-signal gain is given by

$$H = \frac{\frac{(\beta+1)g_{m,11}}{\beta\alpha r_{d,9}} + \frac{g_{m,11}g_{m,13}}{\alpha\delta r_{d,9}}}{-\frac{(\beta+1)g_{m,11}}{\beta\alpha r_{\pi,11}} - \frac{(\beta+1)g_{m,11}}{\beta} - \frac{g_{m,11}g_{m,13}}{\alpha\delta r_{\pi,11}} - \frac{g_{m,11}g_{m,13}}{\delta}} \tag{11}$$

$$Z_{\text{in}} = \frac{r_{d,9}}{1 - \frac{1}{\alpha r_{d,9}} - \frac{H}{\alpha r_{\pi,11}}} \tag{12}$$

$$Z_{\text{out}} = \frac{1}{\left[g_{m,1}g_{m,2}\left(\frac{R_6 r_{\pi,13}}{R_6+r_{\pi,13}}\right) - \frac{\beta+1}{\beta}\right]\left(1 - \frac{R_6}{R_6+r_{\pi,11}}\right)} \tag{13}$$

We can now pick values for R_6 and R_7 that will maximize the input impedance, minimize output impedance, and be as close to unity gain. To achieve this goal, $R_6 = R_7 = 100k\Omega$.

Therefore, the final op-amp transfer function $H(s)$ can be modeled as:

$$H(s) = \left(\frac{Z_{in,\text{AB stage}}}{Z_{in,\text{2nd gain stage}} + Z_{in,\text{AB stage}}}\right) A_{DM,L} A_{\text{2nd gain stage}} A_{\text{AB stage}} \tag{14}$$

After plugging in the chosen values for the resistors and Miller capacitance, the open-loop gain of the op-amp is approximately:

$$H(s) \approx 3 \times 10^6 \tag{15}$$

E. Feedback Network and Oscillator Design

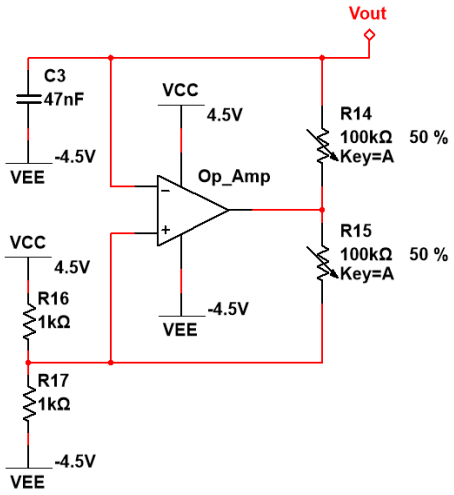

Fig. 4. Feedback Stage Schematic

The feedback network was designed to configure the discrete BJT op-amp as a relaxation oscillator with a target frequency range of approximately 260 Hz to 1040 Hz. The oscillation frequency is determined by the feedback resistances and timing capacitor and is given by:

$$f = \frac{1}{2R_{10}C_3 \ln(\frac{1+\alpha}{1-\alpha})}, \alpha = \frac{R_{17}}{R_{17}+2R_{11}} \tag{16}$$

A capacitor value of 47 nF was selected so that, with 100 kΩ potentiometers, the oscillator would operate in the desired audio range. With $R_{10} = 100k\Omega$ and $R_{11} = 2k\Omega$, the calculated oscillation frequency is approximately 262 Hz, while setting both feedback potentiometers to 100 kΩ yields a frequency of approximately 10.5 kHz. Resistors R_{16} and R_{17} were chosen as equivalent 1 kΩ biasing resistors to set the DC operating point of the feedback network. This provides sufficient tuning range to meet the project frequency requirements.

In addition to controlling frequency, the output amplitude at the inverting node is set by the Schmitt trigger ratio α, since the capacitor voltage oscillates between the two switching thresholds. The resulting peak-to-peak output voltage is given by:

$$V_{out,p-p} = \alpha(V_{OH} - V_{OL}) \tag{17}$$

This shows that the output amplitude scales directly with α. In the ideal case, varying R_{11} with a 100 kΩ potentiometer allows α to change by nearly two orders of magnitude, corresponding to an expected output amplitude control range of up to ≈200X. Even accounting for nonideal effects, this comfortably exceeds the project requirement of a volume range greater than 10X.

F. Summary of Hand Calculated Performance

The key results from the hand calculations used to size the amplifier stages and feedback network are summarized in Tables I and II. These calculations were used to establish expected bias currents, operating points, and oscillator frequency ranges prior to circuit simulation and PCB implementation.

TABLE I
BJT HAND CALCULATION PERFORMANCE SUMMARY

Specification	Req. Spec	Hand Calc.
A_{OL}	$\geq$ 800V/V	≈3 M V/V
f_{-3dB}	≈ 500 kHz ($A_{CL} = 1$)	714kHz
ϕ_m	70°	70°
$V_{out,p-p}$	5.5 V_{p-p} w/o distortion	yes
R_{in}	$\geq 1M\Omega$ ($A_{CL} = 1$)	20k Ω
R_{out}	$\leq 10\Omega$ ($A_{CL} = 1$)	2.9 Ω
P_{diss}	≤80mW ($A_{CL} = 1$)	66 mW

TABLE II
SYNTHESIZER HAND CALCULATION PERFORMANCE SUMMARY

Specification	Req. Spec	Hand. Calc
Frequency of Operation	260-1040 Hz	262-1050 Hz
Output Voltage Range	10X Range	200X Range

III. Simulation Results

This section presents simulation results for the discrete BJT op-amp and the complete audio synthesizer. Simulations were performed using Multisim [1] with a ±4.5 V supply. Unless otherwise noted, the oscillator feedback was disabled to characterize the op-amp and extract the required specifications. The full feedback network was then enabled to verify relaxation oscillator operation and frequency control.

A. DC Operating Point

A DC operating point simulation was performed in Multisim to verify proper biasing of the discrete BJT op-amp prior to AC and transient analysis. The DC bias results, including branch currents and output bias levels, are shown in Fig. 5. With ±4.5 V supplies and the oscillator network disabled, the current mirror generated approximately 200 μA, resulting in a differential pair bias of roughly 200 μA per branch as designed. The differential stage output settled at -3.79 V, while the gain stage NPN emitter voltage was -4.41 V with a 390Ω emitter resistor to V_{EE}, indicating forward-active operation with adequate headroom. Under these conditions, both the gain-stage output (-676 μV) and the class-AB output stage (-129 μV) settled near 0 V, confirming a stable quiescent operating point suitable for symmetric signal swing. Under this same unity-gain, zero-input condition, the op-amp drew approximately 7.38 mA from each supply rail, corresponding to a total quiescent power dissipation of about 66 mW, which is well under the required $P_{diss} \leq 80mW$.

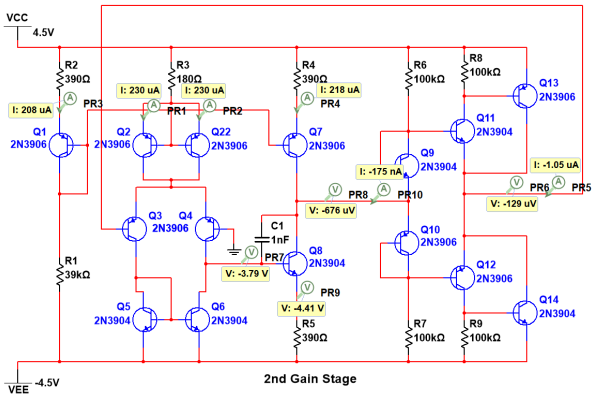

Fig. 5. DC operating point simulation of the discrete BJT op-amp showing branch currents and quiescent bias levels.

B. Open-Loop Gain and Close-Loop Bandwidth

The open-loop gain of the discrete BJT op-amp was evaluated using an AC small-signal simulation with the feedback network removed. The output was probed at the op-amp core output, corresponding to the internal class-AB output stage. As shown in Fig. 6, the amplifier exhibits a low-frequency open-loop gain of approximately 88 dB, which corresponds to a linear gain of about $2.5 * 10^4$ V/V. The closed-loop bandwidth was then evaluated by configuring the op-amp as a unity-gain buffer and performing an AC frequency sweep. The resulting Bode magnitude response is shown in Fig. 7. With 3 nF Miller compensation capacitors applied at the gain stage, the -3 dB bandwidth for $A_{CL} = 1$ was measured to be approximately 900 kHz. This bandwidth meets the design requirements while maintaining stable closed-loop operation.

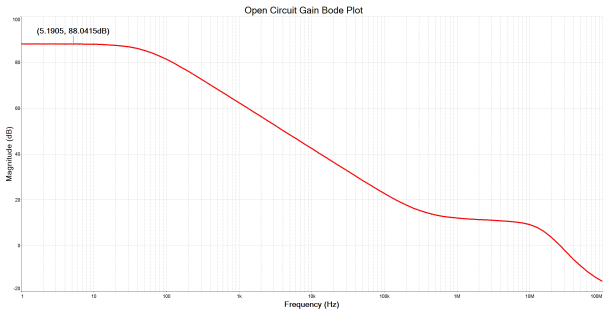

Fig. 6. Simulated open-loop Bode magnitude response of the discrete BJT op-amp used to extract the low-frequency open-loop gain.

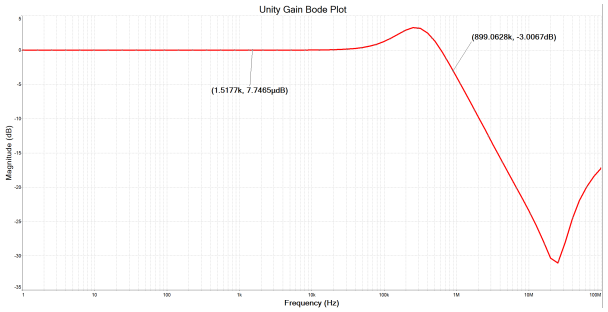

Fig. 7. Close-Loop Unity-gain Bode Magnitude Response of the Discrete BJT op-amp showing -3dB bandwidth.

C. Loop Gain and Phase Margin

Loop gain and phase margin were evaluated using a broken-loop AC analysis. A feedback divider of 22 kΩ and 1 kΩ ($\beta \approx \frac{1}{23}$) was used to reduce the feedback factor and shift the loop-gain crossover to a lower frequency. With this configuration, the loop gain crossed 0 dB at a phase of approximately 70° (measured from an initial 180° reference), corresponding to a phase margin of about 70°. This indicates that the amplifier meets the stability requirement for closed-loop gains of approximately 23 V/V and higher, while unity-gain feedback resulted in insufficient phase margin.

D. Large Signal Transient Response

The large-signal behavior of the discrete BJT op-amp was evaluated in a unity-gain configuration using sinusoidal inputs at 100 Hz and 20 kHz. In both cases, a 2.75 V amplitude signal was applied to the non-inverting input, resulting in an output swing of approximately 5.5 V_{p-p}. The simulated output waveforms, shown in Figs. 9 and 10,

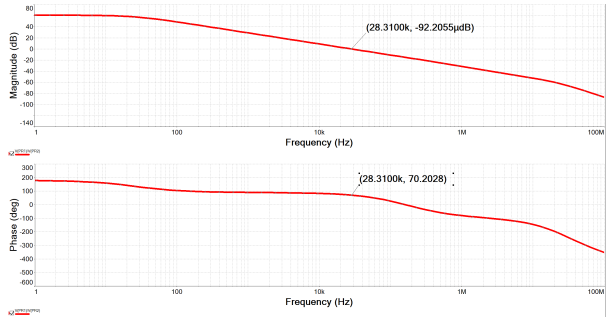

Fig. 8. Simulated loop-gain magnitude and phase of the discrete BJT op-amp using a 22 kΩ / 1 kΩ feedback divider ($\beta \approx \frac{1}{23}$), showing the 0 dB crossover and a corresponding phase margin of approximately 70°.

exhibit no visible clipping or distortion at either frequency. This indicates that the amplifier can support the expected large-signal output swing across the audio frequency range while maintaining stable operation.

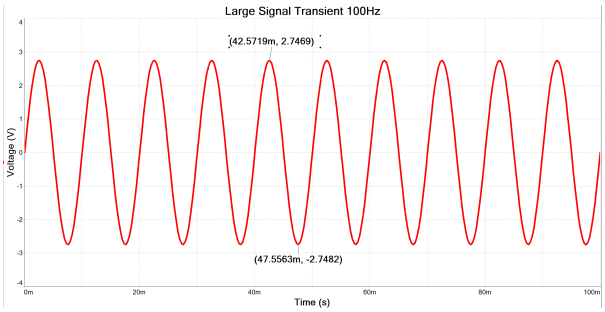

Fig. 9. Simulated large-signal transient response of the discrete BJT op-amp in a unity-gain configuration at 100 Hz, showing an undistorted output swing of approximately 5.5 V_{p-p}.

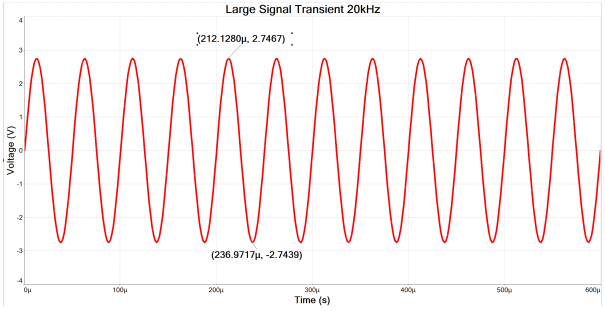

Fig. 10. Simulated large-signal transient response of the discrete BJT op-amp in a unity-gain configuration at 20 kHz, showing an undistorted output swing of approximately 5.5 V_{p-p}.

E. Input and Output Impedances

Input impedance was measured in a unity-gain configuration by injecting a small AC test voltage at the non-inverting input and measuring the resulting input current. As shown in Fig. 11, the input impedance was approximately 16 MΩ at 100 Hz, exceeding the 1 MΩ requirement. Output impedance was measured under closed-loop, passband conditions by injecting a small AC test signal at the output node. The resulting output impedance, shown in Fig. 12, was approximately 3.5 Ω at 1 kHz, meeting the requirement of less than 10 Ω.

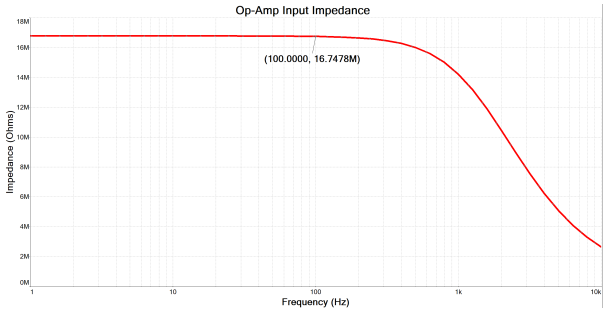

Fig. 11. Simulated input impedance of the discrete BJT op-amp measured in a unity-gain configuration by injecting a small AC test voltage at the non-inverting input at 100 Hz

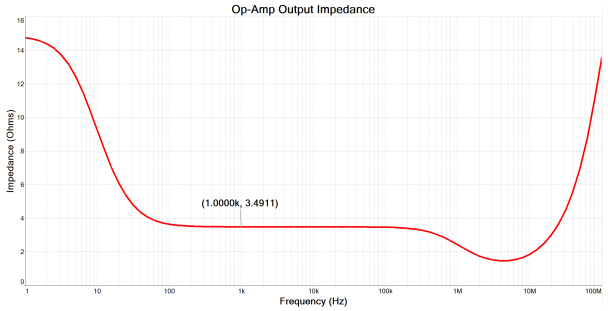

Fig. 12. Simulated output impedance of the discrete BJT op-amp measured by injecting a small AC test signal at the output node with both inputs grounded at 1 kHz.

F. Feeback Network and Oscillation Performance

The oscillator behavior was evaluated using transient simulations of the full synthesizer, including the feedback network, second class-AB buffer stage, and speaker load. Although the final hardware used 10 kΩ potentiometers due to component availability, simulations were performed using the intended 100 kΩ feedback values to verify the original design specifications. With the inverting feedback potentiometer set to 100 kΩ and the non-inverting potentiometer set to 2 kΩ, the circuit produced an oscillation frequency of approximately 215 Hz with an output amplitude of about 1.3 V_{p-p}, as shown in Fig. 13. Setting both feedback potentiometers to 100 kΩ increased the oscillation frequency to approximately 3.3 kHz and reduced V_{p-p} to about 82 mV, as shown in Fig. 14, demonstrating that the synthesizer meets the required frequency range and provides more than a 10X amplitude control.

G. Summary of Simulated Performance

Tables III and IV summarize the key simulated performance metrics of the discrete BJT op-amp and the full audio synthesizer, respectively, providing a concise comparison against the project design requirements.

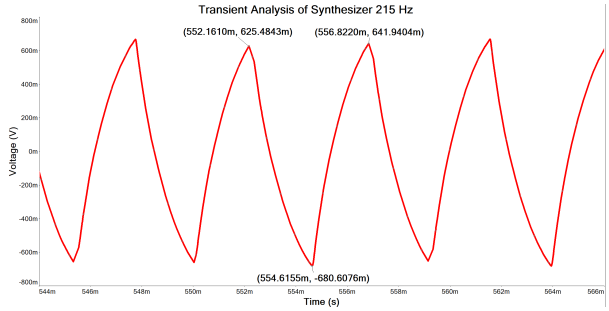

Fig. 13. Transient simulation of the full synthesizer showing low-frequency oscillation (≈215 Hz) with high output amplitude for a low non-inverting feedback resistance.

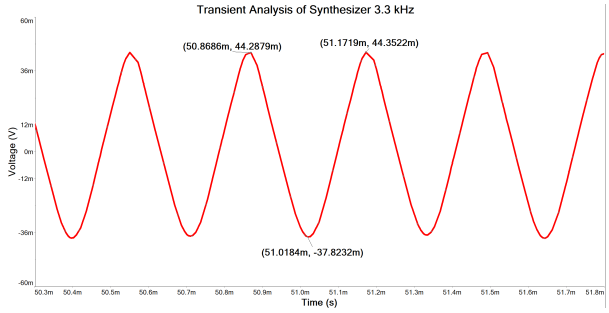

Fig. 14. Transient simulation of the full synthesizer showing higher-frequency oscillation (≈3.3 kHz) with reduced output amplitude for increased feedback resistance.

TABLE III
BJT OP-AMP SIMULATION PERFORMANCE SUMMARY

Specification	Req. Spec	Simulation
A_{OL}	$\geq$ 800V/V	$25 * 10^3$ V/V
f_{-3dB}	$\approx$ 500 kHz ($A_{CL} = 1$)	900 kHz
ϕ_m	70°	70° (k=$\frac{1}{23}$)
$V_{out,p-p}$	5.5 V_{p-p} w/o distortion	yes
R_{in}	$\geq 1M\Omega$ ($A_{CL} = 1$)	16 MΩ
R_{out}	$\leq 10\Omega$ ($A_{CL} = 1$)	3.5 Ω
P_{diss}	$\leq$80mW ($A_{CL} = 1$)	66 mW

TABLE IV
FULL SYNTHESIZER SIMULATION PERFORMANCE SUMMARY

Specification	Req. Spec	Simulation
Frequency of Operation	260-1040 Hz	215-3300 Hz
Output Voltage Range	10X Range	15.8X Range

IV. EXPERIMENTAL DATA

This section presents the measured performance of the fabricated audio synthesizer PCB and compares the results to the expected behavior from hand analysis and simulation. During hardware implementation, minor component substitutions were made based on availability and testing considerations, including the use of 10 kΩ feedback potentiometers and a larger Miller compensation capacitor than originally calculated. Despite these changes, the circuit operated reliably and met the primary project specifications. The following subsections summarize the measured oscillation frequency, output amplitude control, and overall system behavior.

A. Experimental Set up

Measurements were performed using an Analog Discovery 2 (AD2) [2] for signal generation and probing. Jumpers on the PCB were used to isolate the discrete BJT op-amp from the full synthesizer when testing amplifier-level performance. In this configuration, the op-amp was set to unity gain ($A_{CL} = 1$), with external signals injected at the non-inverting input and the output measured through a dedicated jumper node. Oscillation frequency and output amplitudes were measured from time-domain waveforms using the AD2 oscilloscope.

B. Measured Oscillation Frequency

For experimental oscillator testing, both feedback paths were connected and the potentiometers were attached to the inverting and non-inverting inputs. Due to jumper availability, measurements were taken at the node preceding the second class-AB output stage. Stable oscillation was observed over a frequency range from approximately 164.5 Hz at the low setting to 1662.7 Hz at the high setting. Attempts to push beyond this range resulted in unstable behavior. These measurements confirm that the fabricated system produced audible oscillations over a wide frequency range consistent with the intended synthesizer operation.

C. Measured Output Amplitude and Unity-Gain Behavior

With the op-amp isolated and configured for unity gain, a sinusoidal input of 2.75 V amplitude was applied to the non-inverting input. The measured output exhibited a stable peak-to-peak voltage of approximately 5.45 V, consistent with unity-gain operation. Attempts to experimentally vary the output amplitude using the non-inverting feedback potentiometer were unsuccessful, as small adjustments often caused the oscillation to collapse. As a result, precise experimental characterization of the volume control range was not possible, although stable output operation was confirmed at fixed potentiometer settings.

D. Power Dissipation

With the op-amp configured for unity gain and the non-inverting input grounded, a supply current of approximately 7.79 mA was measured using the AD2. This corresponds to a quiescent power dissipation of approximately 70.1 mW during steady-state operation.

E. Summary of Measured Performance

Tables V and VI summarizes the key experimentally measured performance metrics of the discrete op-amp and audio synthesizer

TABLE V
BJT OP-AMP MEASURED PERFORMANCE SUMMARY

Specification	Req. Spec	Simulation
f_{-3dB}	$\approx$ 500 kHz ($A_{CL} = 1$)	100 kHz
$V_{out,p-p}$	5.5 V_{p-p} w/o distortion	yes
P_{diss}	$\leq$80mW ($A_{CL} = 1$)	70.1 mW

TABLE VI
FULL SYNTHESIZER MEASURED PERFORMANCE SUMMARY

Specification	Req. Spec	Simulation
Frequency of Operation	260-1040 Hz	165-1660 Hz
Output Voltage Range	10X Range	N/A

V. DISCUSSION AND CONCLUSIONS

This project progressed through hand analysis, simulation, and experimental implementation, with several adjustments made as the design moved into hardware. Overall, the final circuit behaved in line with expectations from simulation and successfully demonstrated a fully discrete BJT-based op-amp used in an audio synthesizer. The main project goal of generating audible oscillations with controllable frequency was achieved, and the op-amp operated correctly in unity gain with appropriate output swing and power dissipation. While the experimentally measured frequency range was smaller than what was predicted in simulation, this difference can be explained by component tolerances, loading effects, and the use of 10 kΩ potentiometers in the final hardware instead of the originally designed 100 kΩ values.

One significant design change involved the Miller compensation capacitor. Although a much smaller value was calculated during hand analysis, a larger Miller capacitor was chosen during experimental testing because it resulted in more stable operation and made frequency adjustment more predictable when using the lower-value potentiometers. While this reduced the overall bandwidth compared to simulation, it did not impact the intended audio-frequency operation and ultimately improved usability. Independent amplitude control, however, was not successfully achieved in hardware. Adjusting the amplitude control potentiometer often caused the oscillation to collapse, likely due to interaction between the feedback networks, loading at the non-inverting input, and limited drive capability of the output stage. In a future design, this issue could be addressed by further isolating the amplitude control from the oscillator loop, adding buffering at the non-inverting input, or redesigning the output stage to better drive low-impedance loads. Despite these limitations, the project provided valuable hands-on experience with discrete analog design and highlighted the tradeoffs between theoretical design and real-world implementation.

REFERENCES

[1] *Multisim*, National Instruments. [Online]. Available: https://www.multisim.com/.

[2] *Analog discovery 2*, Digilant. [Online]. Available: https://digilent.com/reference/test-and-measurement/analog-discovery-2/start.

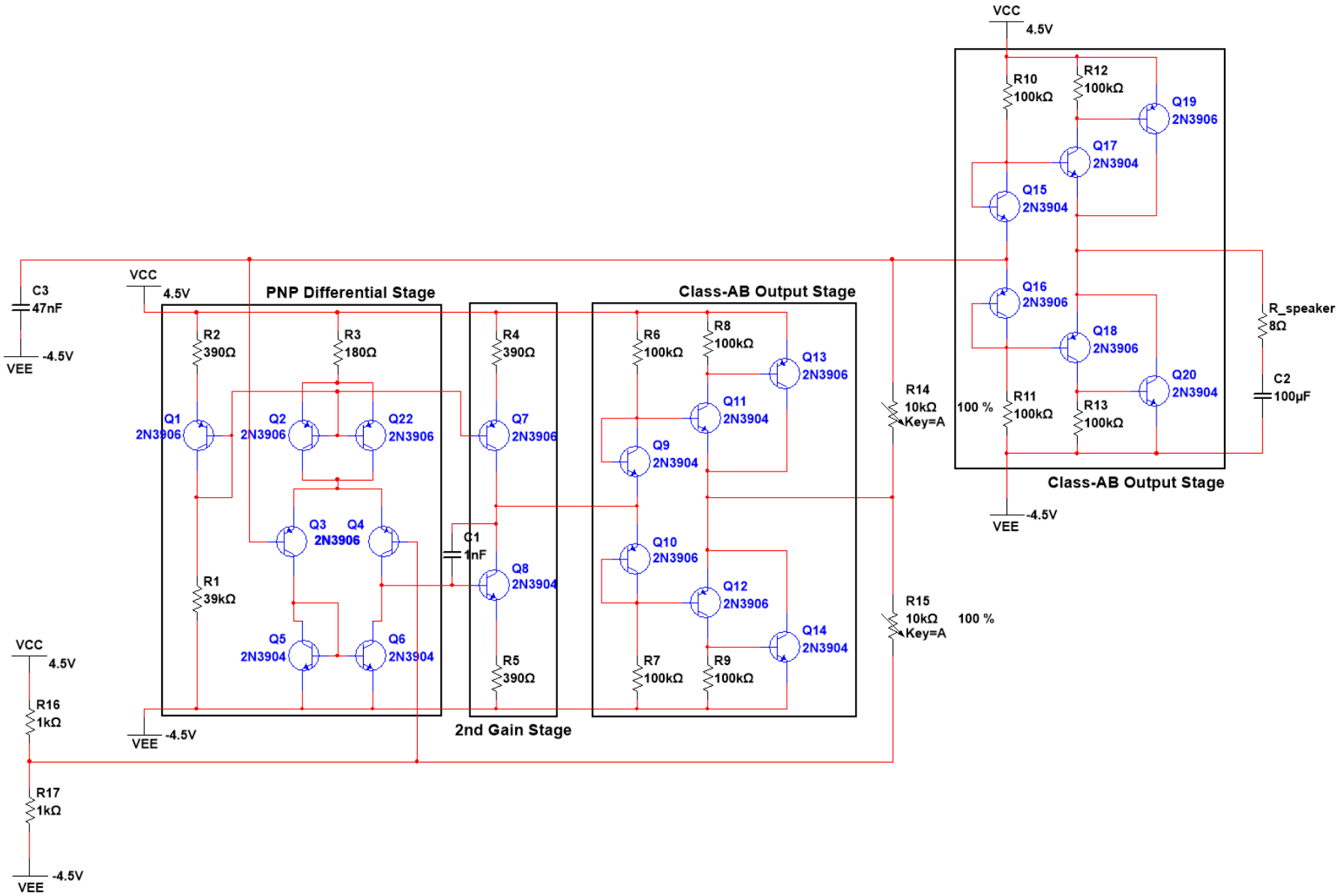

Fig. 15. Full Schematic of the Audio Analyzer Circuit